REMARKS

This Amendment is responsive to the Office Action identified above, and is responsive in any other manner indicated below.

SUPPLEMENTAL REISSUE OATH/DECLARATION

Regarding the page 2 rejection of claims 1-63 concerning a defective declaration, Applicant respectfully submits that a supplemental reissue oath/declaration will be filed at the end of prosecution when all other issues/rejections have been resolved and no more claim or other changes are to be made. Accordingly, when the supplemental reissue oath/declaration becomes the only issue barring allowance of the application, the Examiner is invited to call the undersigned at the local Washington, D.C. telephone number of 703-312-6600 to provoke accelerated preparation/filing of the final supplemental reissue oath/declaration to move the application to allowance.

PENDING CLAIMS

Appropriate claims have been amended, canceled and/or added (without prejudice or disclaimer) in order to adjust a clarity and/or (correcting improper) renumbering of Applicant's claimed invention. At entry of this paper, Claims 1-36 and 50-76 will be pending for further consideration and examination in the application.

RENUMBERING OF CLAIMS

With regard to the objection regarding the prior improper renumbering of claims (as set forth within the "Numbering of Claims" section), the claims have been returned to their original proper numbering, and reissue status identifiers added. Reconsideration and withdrawal of the objection, are respectfully requested.

REJECTION UNDER '112, 1st PAR. - TRAVERSED

Claims 45-47 and 50-59 have been rejected under 35 USC '112, first paragraph, as failing to comply with the written description requirement. Ones of Applicant's claims have been clarified to address some of the 112, 1st para. concerns. Regarding other ones of the 112, 1st para. concerns, Applicant respectfully reiterates the following Office Action concern(s) and follows with Applicant's traversal:

> Office Action Concern:
> Concerning claims 45, an adhesive layer is not provided on each of said suspension leads which is located under said semiconductor chip. Please see the Spec in column 8, lines 51-65.

Applicant's Traversal: Applicant's present claim 45 is directed to the structure as shown in the example FIGS. 13 and 17 which clearly show that an adhesive layer 15 is provided at a central position of the chip mounting portion 3, but is not provided at the suspension leads 4 under the chip. The description (Column 8) referred to by the Examiner are directed to another embodiment.

> Office Action Concern:
> Concerning claim 47, there is no support for "thermosetting resin". Please see the Spec in column 10, lines 11-14.

Applicant's Traversal: Applicant respectfully directs attention to column 8, lines 33-35, where written description support can be found.

> Office Action Concern:
> Concerning claim 50, the Spec does not teach only two suspension leads...

Applicant's Traversal: Applicant respectfully submits that support for two leads is clearly shown in example FIG. 32 showing two intersecting leads (widened at a central portion thereof).

> Office Action Concern:
> Concerning claim 51, the Spec does not teach only two suspension leads intersecting at right angles...

Applicant's Traversal: Applicant respectfully submits that support for two leads is clearly shown in example FIG. 32 showing two intersecting leads (widened at a central portion thereof), which intersect at right angles.

> Office Action Concern:
> Concerning claims 52 and 54, the Spec does not support "tetragonal shape". Please see amendment filed of July 6, 1995 in parent application.

Applicant's Traversal: Webster's II New College Dictionary, copyright 1999, at page 1141, defines a "tetragon" as "a four-sided polygon". It is respectfully submitted that IC chips are almost universally provided as "tetragonally shaped". Applicant's FIG. 29, for example, has illustration of a "tetragonally-shaped" IC. Accordingly, it is respectfully submitted that "tetragonally shaped" is supported, and well known by persons skilled in the art. Even if the word "tetragonally" is not written within the specification, MPEP 2163 (directed to "written description" guidelines) itself, explicitly states "...**there is no *in haec verba* requirement**..." (i.e., "in the same words" requirement) with respect to "written description", and continues to state simply that

"...newly added claim limitations must be supported in the specification **through express, implicit, or inherent disclosure**."

As the foregoing is believed to have addressed all '112, 1st paragraph concerns, reconsideration and withdrawal of the '112, 1st paragraph rejection are respectfully requested.

ALLEGED IMPROPER BROADENING - TRAVERSED

Claims 15-36 have been rejected under 35 USC 251 as being broadened within a reissue application filed allegedly outside the two year statutory period. Traversal is appropriate, because the parent patent 5,637,913 issued 10 June 1997, and the first reissue (in the present family of reissues) was filed as a broadening reissue on 09 June 1999. Further, as explained within MPEP 1412.03 (IV), once a broadening reissue is filed within the two year statutory period, that Applicant is allowed to submit additional broadening claims BEYOND the two year statutory period, even within subsequent reissue continuations/divisionals filed later than the two year statutory period. Reconsideration and withdrawal of the rejection, are respectfully requested.

"PROVISIONAL" DOUBLE-PATENTING

It is respectfully noted that the present double-patenting rejection is only a "provisional" double-patenting rejection. As a result, Applicant respectfully submits a traversal, but refrains from commenting further on a substance of the rejection at this time, until an actual double-patenting rejection is made.

EARLIEST-FILED "PROVISIONALLY-REJECTED" APPLICATION

It is respectfully noted that this is the earliest-filed application of the applications involved in the present "provisional" double-patenting rejection. MPEP 804 states (in relevant part) that: "If a "provisional" nonstatutory obviousness-type double patenting (ODP) rejection is the only rejection remaining in the earlier filed of the two pending applications, while the later-filed application is rejectable on other grounds, the examiner should withdraw that rejection and permit the earlier-filed application to issue as a patent without a terminal disclaimer." Withdrawal of the "provisional" double-patenting rejection, and allowance of the present (earliest-filed) application, are respectfully requested.

RECAPTURE REJECTION - TRAVERSED

For the purposes of the following discussions, the previously-pending proper claim numbers will be used to identify the specific claims now properly renumbered herein.

The recapture rejection of Claims 63-72 as set forth within the section numbered "7" on page 6 of the Office Action (and/or within prior Office Actions) is respectfully traversed.

It is respectfully submitted that the standing recapture rejection appears to be based upon old case-law, in that the rejection is improper and a number of old legal cases are cited in support of the recapture rejection. More particularly, in contrast to the cited older cases, *ex parte Eggert*, Appeal No. 2001-0790, decided 29 May 2003 provides the legal analysis that should be applied/followed for recapture analysis. The Eggert discussions/analysis

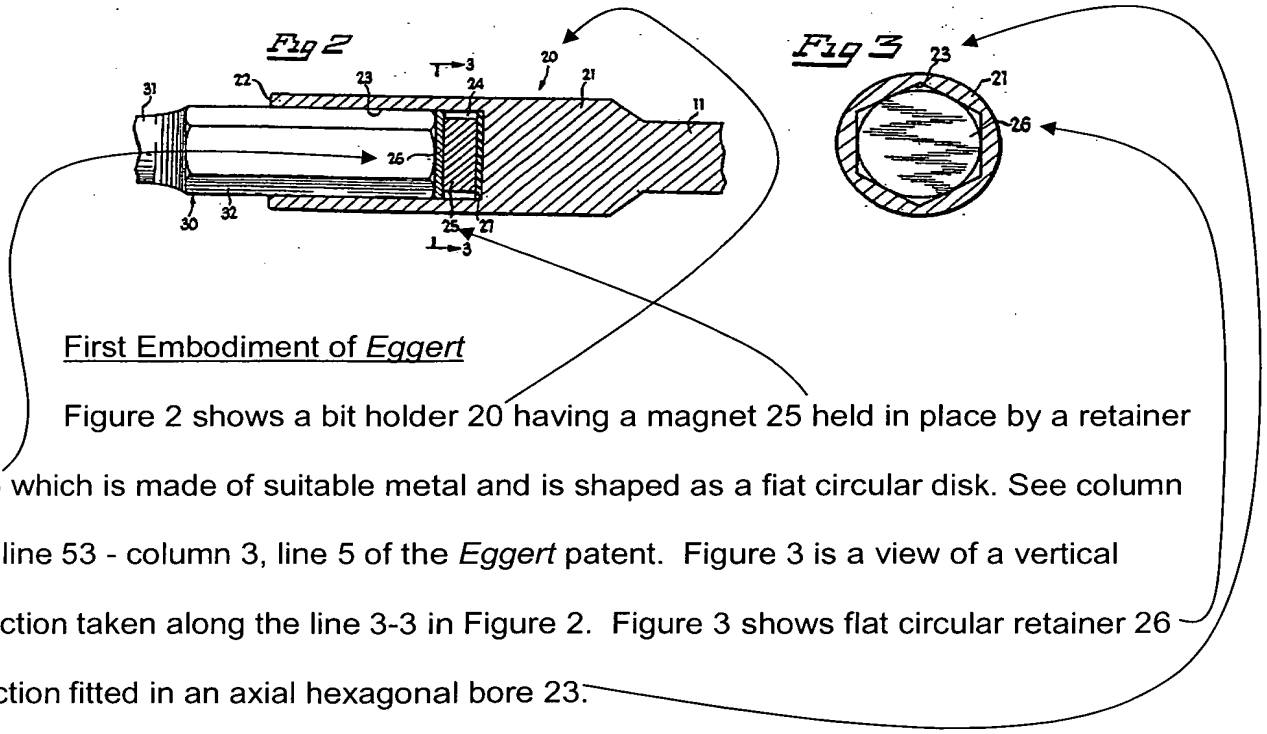
provided in Applicant's prior papers has been further elaborated upon in the following.

ex parte Eggert discussion:

More particularly, the relatively-recent precedential USPTO Board opinion of *ex parte Eggert*, Appeal No. 2001-0790, was decided 29 May 2003, concerning US Patent No. 5,577,426. In such case, the Board **REVERSED** the Examiner's attempt to apply recapture to reject the application. Background teaching of the *Eggert* opinion is relevant for understanding of traversal/rebuttal of the present rejection in Applicant's application.

The invention in *Eggert* was related to a magnetic bit holder. Two embodiments were at issue in *Eggert*'s appeal; such two embodiments are briefly described on the next two pages.

The first embodiment is shown in *Eggert*'s FIGS. 2 and 3 as follows:



First Embodiment of *Eggert*

Figure 2 shows a bit holder 20 having a magnet 25 held in place by a retainer 26 which is made of suitable metal and is shaped as a fiat circular disk. See column 2, line 53 - column 3, line 5 of the *Eggert* patent. Figure 3 is a view of a vertical section taken along the line 3-3 in Figure 2. Figure 3 shows flat circular retainer 26 friction fitted in an axial hexagonal bore 23.

The second embodiment is shown in *Eggert*'s FIGS. 4, 5 and 6 as follows:

Fig 4

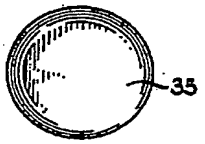


Fig 5

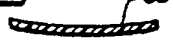
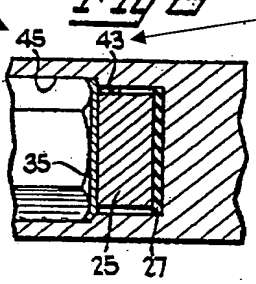


Fig 6



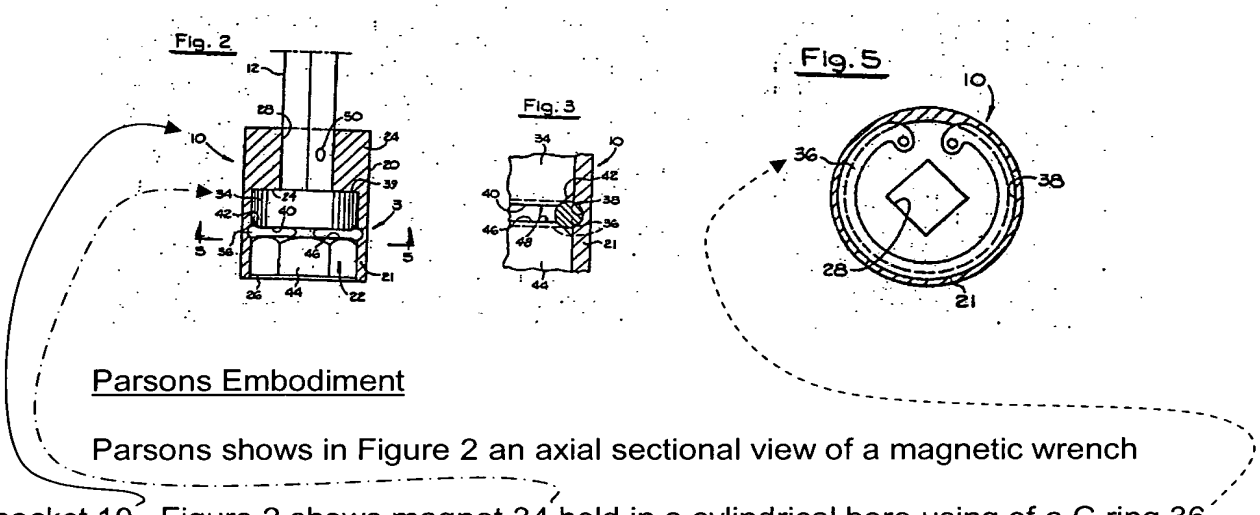
Second Embodiment of *Eggert*

In the second embodiment, an alternative bit holder is shown which is similar to bit holder 20 in the first embodiment, except the nature of the bore and retainer are different. More specifically, the bit holder of Figure 6 has a cylindrical body which has a circularly cylindrical axial bore 43 in addition to a hexagonal bore 45. See column 3, lines 48-55.

Figure 6 shows that magnet 25 is dimensioned to fit freely in the cylindrical bore 43 and is held in place by a retainer 35 friction fitted in the hexagonal bore 45. See column 3, lines 59-64. Figures 4-6 show that the retainer 35 is formed of suitable plastic material and generally bowl-shaped and convex toward the magnet. See column 3, lines 35-47.

Eggert's original independent claim 1 recited the language "retaining structure in contact with the outer surface of said magnet and interference fitted in said bore to retain said magnet in said bore." Original claim 1's limitations, thus, encompassed *Eggert*'s both first and second embodiments.

In a rejection, the *Eggert* Examiner applied Parsons, US Patent No. 4,663,998 (shown as follows), for a teaching of the broadly claimed retaining structure.



Parsons Embodiment

Parsons shows in Figure 2 an axial sectional view of a magnetic wrench socket 10. Figure 2 shows magnet 34 held in a cylindrical bore using of a C ring 36. See column 1, lines 35-65, of Parsons. Figure 3 of Parsons is a large scale sectional view of a portion of Figure 2 indicated by arrow 3. Figure 3 shows the C ring 36 releasably held in a peripheral groove 38 formed in the wall 21. See column I, lines 29 and 30, and lines 60-65. Figure 5 of Parsons shows a sectional view taken at line 5-5 of Figure 2 and shows C ring 36 releasably held in peripheral groove 38 formed in the wall 21. See column 1, lines 34 and 35, and lines 60-65. Thus, Parsons describes what in essence is a third (cited prior art) embodiment covered by the language of *Eggert*'s original claim 1.

In response to the Examiner's rejections applying Parsons to the claimed retaining structure, *Eggert*'s applicant eventually rewrote non-art-rejected dependent claim 6 into independent form. Claim 6 added the limitation of "said retaining member being generally bowl-shaped and convex toward said magnet" to claim 1. This claim language corresponds only to the second embodiment disclosed in Figures 4, 5 and 6. That is, note that such non-generic language excluded *Eggert*'s disclosed first embodiment which is a flat, circular metal disk 6. The Examiner entered the amendment and appeared to allow the application on a basis of such "bowl-shaped and convex" feature/limitations, and the *Eggert* patent issued.

Attached herewith ia an appendix sheet titled "Eggert Analysis". A right-hand column of such "Eggert Analysis" sheet reiterates the issued claim 1, with gray highlighting within such claim indicating the feature/limitations which appeared to gain allowance. Again, remember that such overly-narrow features/limitations did NOT cover Applicant's first (FIGS. 2-3) flat, circular metal disk 6 embodiment.

Subsequently (i.e., post-issuance), *Eggert*'s applicant attempted to correct the overly-narrow claim limitation by reissue. More particularly, *Eggert*'s applicant presented new reissue independent claims 15 and 22 which were of sufficient scope to not only cover both of their disclosed FIGS. 2-3 (flat metal disk) and FIGS. 4-6 (bowl-shaped, convex disk) embodiments, but also distinguish over the C ring of Parsons. For example, the new language of claim 15 (**shown in the center column of the attached "Eggert Analysis" sheet**) reads "a discrete retaining member friction fitted in said bore outboard of said magnet and substantially covering said outer surface of said magnet to retain said magnet in the bore." The scope of this language included both the first and second embodiments of *Eggert*'s invention, and

as recognized by the *Eggert* Examiner, was free of the prior art of record. But note from viewing the attached Eggert analysis sheet, that such claim was attempting to delete the "bowl-shaped and convex" feature/limitations (see encircled portions) which were instrumental in gaining allowance.

Eggert's application (like the present application), was then rejected based on the "reissue recapture rule". On a first round of USPTO appeal, the *Eggert* Examiner asked an initial 3-person USPTO Board to impose a *per se* rule of reissue recapture to prevent the *Eggert* Appellant from retreating from any claim limitation determined to have secured allowance of the original patent. The Examiner **LOST (i.e., was reversed)** in the first round of appeal. After losing upon decision of a 3-person Board, the *Eggert* Examiner then requested and got a **second** round **full-Board-panel** reconsideration and urged the full Board to reverse the prior decision and to adopt the *per se* rule. The **full-Board also rejected the *per se* rule**, reversing the examiner to ultimately allow the *Eggert* Appellant to use reissue **to retreat from the original overly limiting claim limitations**.

The Eggert decision may be interpreted as follows. More particularly, attention is directed again to the attached "Eggert Analysis" sheet, wherein circles or Venn diagrams may be used in explanation/analysis of recapture. Attention is directed to the Venn diagram at the top of the "Eggert Analysis" sheet. The issued claim (right-hand column of the "Eggert Analysis" sheet) has a narrowest scope as shown representatively by the smaller (inner) Venn diagram circle. In contrast, the surrendered claim (left-hand column of the "Eggert Analysis" sheet) not having the allowable features/limitations (of the issued claim), has the broadest scope as shown representatively by the larger (outer) Venn diagram circle. The Eggert decision

states that the **grayed Venn diagram area** represents **intermediate** claim features/limitations/scope which have **NOT YET BEEN CONSIDERED BY THE EXAMINER DURING PROSECUTION, AND BECAUSE IT HAS NOT BEEN CONSIDERED, IT HAS NOT BEEN SURRENDERED BY APPLICANT**. That is, since it has **not been considered/surrendered**, a reissue Applicant can freely claim within this grayed area **WITHOUT VIOLATING RECAPTURE**.

Note with respect to reissue claim 15 (center column) on the "Eggert Analysis" sheet, that the full Board reversed the examiner's recapture rejection concerning the disputed limitations (see circled portion of the center and right columns of "Eggert Analysis" sheet), and allowed Eggert's reissue applicant to actually back away from the features/limitations which gained the allowance of the original issued claim. The important teaching to comprehend, is that, as long as a reissue claim is of **intermediate scope** (grayed Venn diagram area) between the surrendered claim and issued claim, then the reissue claim **DOES NOT VIOLATE THE RECAPTURE RULE**. (As will be seen ahead, Applicant's reissue claims are likewise of intermediate scope between the surrendered and issued claims.)

The effect of the Eggert decision was that *Eggert*'s Appellant was not limited to the "retaining member being generally bowl-shaped and convex toward said magnet" limitations of the patented claims. Instead, *Eggert*'s applicant was able to obtain intermediate new reissue independent claims 15 and 22 which recited, for example, "a discrete retaining member friction fitted in said bore outboard of said magnet and substantially covering said outer surface of said magnet to retain said magnet in the bore." The scope of this language included both of *Eggert*'s FIGs. 1-2 and FIGs. 4-6 embodiments. **Thus, to summarize, Reissue applicants are NOT**

frozen at the scope of patented claims, but instead, Reissue may be used to pursue intermediate scope claims to supplement and/or broaden erroneous (e.g., overly restrictive) claims. This Board finding makes sense in that, if a *per se* reissue recapture rule were always applied/applicable, such would totally negate any need for a reissue procedure within the USPTO.

Added Claims 73-76:

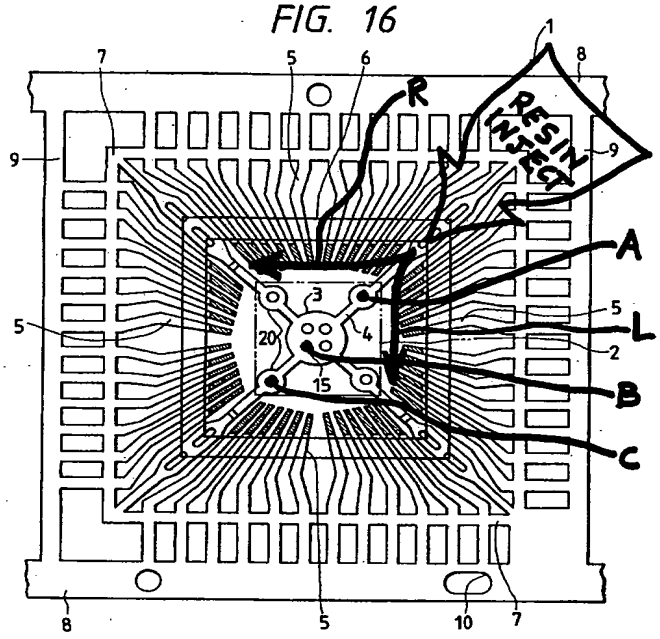
Discussion turns now to the present application at hand. Presently added independent claims 73-76 will logically be discussed first to preclude application of any "*per se* reissue recapture rule" with respect to such new claims. More particularly, from a historical perspective, in reviewing the independent claims during reissue review for the present Amendment, it has been determined that the patented claim limitations of (*e.g.*, see claim 1) "said semiconductor chip is fixed to a part of **each** of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip", are **unnecessarily restrictive in scope**, and thus are an "error".

More particularly, during prosecution of the parent patent, it was argued the advantage of the foregoing was that "adhesion of the semiconductor chip to the leadframe can be sufficiently provided so as to prevent a shifting of the semiconductor chip during manufacturing." However, it has subsequently been realized that it is NOT absolutely necessary to fix (*e.g.*, adhere) a semiconductor chip to **each** suspension lead (i.e., all suspension leads) in order to prevent shifting.

More particularly, all that may be required is that the semiconductor chip be minimally fixed at **two shift-preventing positions separated from each other** to

prevent shifting during manufacturing (*e.g.*, resin encapsulation). A modified version of Applicant's FIG. 16 will be used in example explanation as follows:

FIG. 16



Applicant's FIG. 16 (w/explanatory marked modifications)

More particularly, as one example, assume that resin in injected (during a resin encapsulation operation) from a FIG. 16 die corner opposing a point A, in a general direction as shown by the large arrow above. Such injected resin may tend to flow along one of the suspension leads (note that there are 4 suspension leads in this example), and then upon arriving at a die corner opposing the point A, the injected resin may split and equally flow in right R and left L halves (see above FIG) down opposing sides of the die. Such splitting/equalized flow may cause offsetting (*i.e.*, balanced) torque pressures being applied to the die on opposing sides of the suspension lead. Since balanced torque pressures are applied, no significant torque pressures are applied to twist the die off of the lead frame carrier. In such a

situation, fixing the die 2 minimally at two separated positions (*e.g.*, at darkened locations A and B (or B and C)) may very well be sufficient to prevent shifting.

Since it is NOT absolutely necessary to fix (*e.g.*, adhere) a semiconductor chip to **each** suspension lead (i.e., all suspension leads) in order to prevent shifting, again, it is respectfully submitted that Applicant's patented claims were/are **unnecessarily and overly narrow**. In an attempt to remedy such narrowness, Applicant's new independent claims 73-76 substantially parallel the patented independent claims 1, 11, 13 and 14, respectively, but retreat from the overly-restrictive "each" language. That is, recited claims 73-76's (*e.g.*, independent claim 73's) chip is "fixed to said chip mounting portion by adhesive", and is also "fixed to a part of ~~each~~ **at least one** of said suspension leads by adhesive". Thus, note that such claims in effect recite a semiconductor chip fixed at **two (shift-preventing) positions (i.e., a "chip mounting portion" and "at least one ...suspension lead") separated from each other** to prevent shifting during manufacturing (*e.g.*, during the resin encapsulation operation).

None of the references taken alone or in combination would have disclosed or suggested Applicant's combination of features/limitations as recited in claims 73-76. That is, the chip is "fixed to said chip mounting portion by adhesive", and is also "fixed to a part of **at least one** of said suspension leads by adhesive", *i.e.*, at **two shift-preventing positions separated from each other** to prevent shifting during manufacturing (*e.g.*, during the resin encapsulation operation). Such arrangement and the fact that the adhesion locations are separated from each other is also advantageous in that it MINIMIZES an adhesion area used on a back of the chip, and thus water vapor reflow cracking is correspondingly MINIMIZED.

Turning now to recapture analysis via an Eggret-type Venn diagram analysis, attention is directed again to the attached "Present Application Analysis" sheet, where again, circles or Venn diagrams may be used in explanation/analysis of recapture. Attention is directed to the Venn diagram at the top of the sheet. The issued claim (right-hand column of the sheet) has a narrowest scope as shown representatively by the smaller (inner) Venn diagram circle. **Gray highlighting** within such claim indicates the feature/limitations pointed to by the Examiner as reasons for allowance. In contrast, the surrendered claim (left-hand column of the sheet) not having the allowable features/limitations (of the issued claim), has the broadest scope as shown representatively by the larger (outer) Venn diagram circle.

The center column includes a reiteration of present example reissue claim 73. Circled portions of the center and right columns indicate features/limitations which are changed with respect to the issued claim and reissue claim 73. Given that the "each of" features/limitations within issued claim 1 are narrower than the "at least one of" features/limitations of reissue claim 73, and given that surrendered claim 25 (i.e., corresponding to issued claim 1) does not contain such features/limitations, clearly the "at least one of" features/limitations are of **intermediate in scope**. Clearly, example claim 73 has a scope within the **grayed Venn diagram area**.

As explained above, the Eggert decision states that the **grayed Venn diagram area** represents claim features/limitations/scope which have **NOT YET BEEN CONSIDERED BY THE EXAMINER DURING PROSECUTION, AND BECAUSE IT HAS NOT BEEN CONSIDERED, IT HAS NOT BEEN SURRENDERED BY APPLICANT**. That is, a reissue Applicant can claim within this grayed area **WITHOUT VIOLATING RECAPTURE**. Thus, it is respectfully

submitted that Applicant's example reissue claim 73 (and similar claims) do not violate recapture, and thus the recapture rejection is improper and should be withdrawn.

In conclusion, it is respectfully submitted that such claims 73-76 (*i.e.*, like the *Eggert* opinion discussed above), correct the above-discussed overly-narrow claiming error (*e.g.*, of independent claim 1), while at the same time sufficiently distinguishing over the art of record.

Claims 63-67:

Recapture rebuttal now continues with further discussions regarding **independent claim 63** (and claims 62-67 dependent therefrom). More particularly (like the above-discussed new renumbered claims), clarified claim 63 also contains limitations equivalent to a situation where the rear surface of the semiconductor chip is fixed to the first and second suspension leads **by an adhesive at at least two shift-preventing positions separated from each other**. For a proper understanding of claim 63, an initial discussion of patented independent claim 1 may be helpful/appropriate, and hence, such discussion is now provided herewith as follows.

More particularly, independent claim 1 recites "a leadframe having: a chip mounting portion for mounting said semiconductor chip; suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads." That is, note that there is both a **mounting portion** and **suspension leads**. Subsequent review of such claim related to the present reissue process revealed that such claim 1 limitations may be

too narrow. More particularly, a potential infringer might (in a bid to avoid infringement) leave out the "chip mounting portion" or "flag" (as known in the art), and then attempt an argument that the claimed "chip mounting portion" covered "flagged" chip supporting arrangements, but did not cover "flag-less" chip supporting arrangements. Not covering a "flag-less" arrangement is another error within the present patent, which is attempted to be corrected by the present Reissue application.

Description/understanding of "flagged" verses "flag-less" may be helpful in understanding the present situation; hence, attention is now directed to the following Applicant's FIGS. 31-32 for a "flagged" verses "flag-less" explanation:

FIG. 31

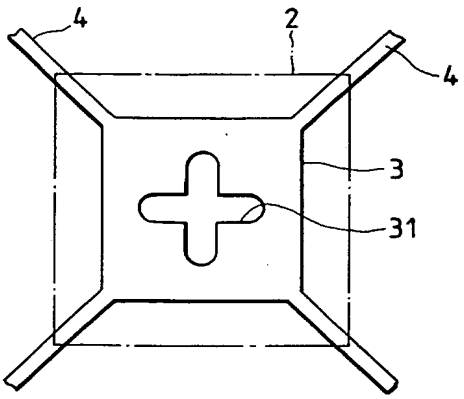
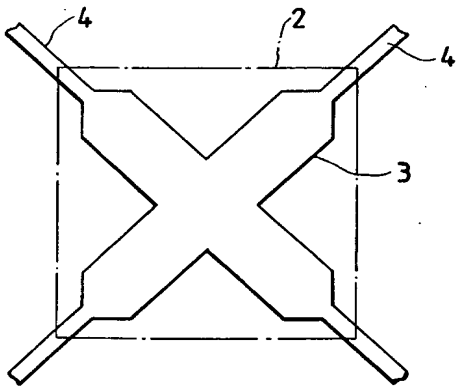


FIG. 32



Applicant's FIGS. 31 and 32

Applicant's FIG. 31 represents a "flagged" arrangement as is understood by persons skilled in the art (*i.e.*, note that the rectangle in FIG. 31 resembles a flag; in the art, the flag may also be circular as will be shown ahead); in contrast, Applicant's FIG. 32 represents a "flag-less arrangement.

"Flag" and "flag-less" terminology is known in the art, as Djennas *et al.*'s (U.S. Patent No. 5,327,008; of record) illustrates/describes a plurality of differing die-supporting arrangements, including rectangular mini-flag, circular mini-flag AND flag-less arrangements. Djennas *et al.*'s column 6, lines 14-21, describes that Djennas *et al.*'s "FIG. 4 illustrates, in a top-down plan view, portions of a lead frame 40 having such a **mini-flag** 42. Mini-flag 42 is kept smaller in area than a semiconductor die (illustrated in phantom as line 44) to keep the total interface area between the mini-flag and a plastic encapsulation material (not illustrated) smaller than in conventional devices." Next, Djennas *et al.*'s column 6, lines 45-48, describes that the above-reproduced "...FIG. 6 portions of a lead frame 50 (only partially illustrated) can include a **round mini-flag** 52 to support a large die (illustrated in phantom as line 54)."

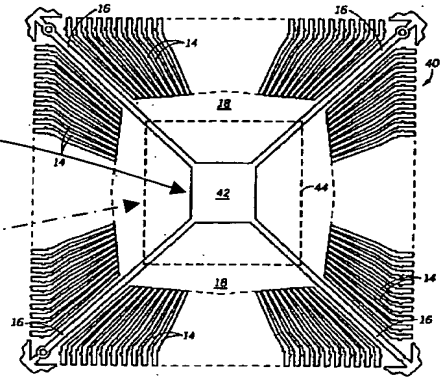


FIG. 4

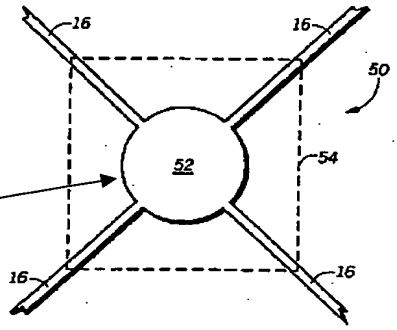


FIG. 6

Most importantly, and most relevant to the present situation, Djennas *et al.*'s column 4, lines 35-37, describes that Djennas *et al.*'s "...FIG. 1 [reproduced herewith] device 10 **does not employ a flag.** Instead, die 20 rests on tie bars 16." Accordingly, the Djennas *et al.* FIG. 1 arrangement is a "flag-less" arrangement somewhat similar to Applicant's FIG. 32 (re-illustrated ahead).

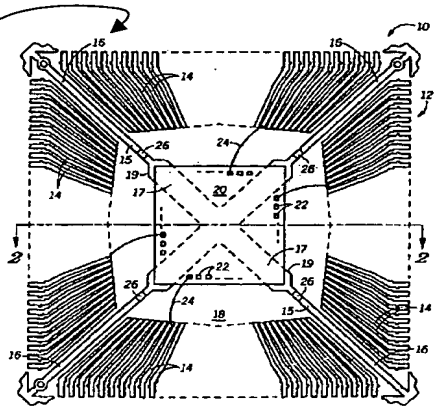
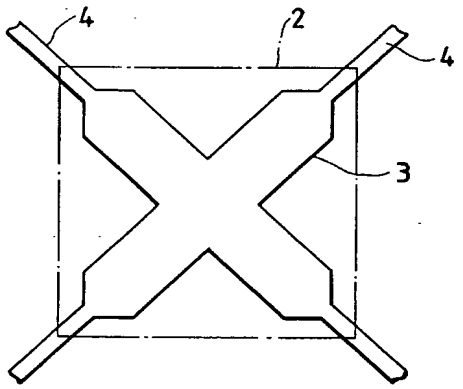


FIG. 1

Accordingly, with the above understanding of "flagged" verses "flag-less", Applicant's present independent claim 63 (and claims dependent therefrom) is directed toward claiming a semiconductor device utilizing a "flag-less" (Applicant's FIG. 32) arrangement. In terms of claim features/limitations of interest, independent claim 63 claims: "a lead frame including: a first suspension lead (4) for supporting said semiconductor chip, extending in a first direction; a second suspension lead (4) for supporting said semiconductor chip, extending in a second direction which is different from said first direction, said second suspension lead intersecting said first suspension lead; and ...wherein said semiconductor chip is disposed on and supported by **a flag-less said intersecting portion of said first and second suspension leads,** with said first and second suspension leads being unitarily formed with one another, wherein a width of each of said first and second suspension leads supporting said semiconductor chip at the vicinity of said intersecting portion is wider than that of each said first and second suspension leads at vicinities beyond said semiconductor chip, and widened portions of said first and second suspension leads are smaller than said semiconductor chip." Further, independent claim 63 also has the adhesion features/limitations discussed above with respect to other ones of Applicant's claims, *i.e.*, "wherein said rear surface of said semiconductor chip is fixed to said first and second suspension leads by an adhesive at at least two shift-preventing positions separated from each other."

FIG. 32



To conclude, claim 63 (and claims dependent therefrom) corrects the above-discussed overly-narrow claiming error (*e.g.*, of independent claim 1), while at the same time sufficiently distinguishing over the art of record. That is, none of the references taken alone or in combination would have disclosed or suggested Applicant's combination of features/limitations as recited in claim 63 (or claims 64-67 dependent therefrom). For example, while Djennas *et al.*'s FIG. 1 discloses a "flag-less" arrangement, such FIG. teaches away from Applicant's claim 63 features/limitations of: "wherein a width of each of said first and second suspension leads supporting said semiconductor chip at the vicinity of said intersecting portion is **wider** than that of each said first and second suspension leads **at vicinities beyond said semiconductor chip.**" That is, it is noted that Djennas *et al.*'s FIG. 1 arrangement has "wide" portions that extend **beyond** the Djennas *et al.* chip. [Further, note that Djennas *et al.* is removeable as prior art given that it has an effective filing date of 22 March 1993, whereas Applicant's foreign priority application has a filing date of 27 March 1992.]

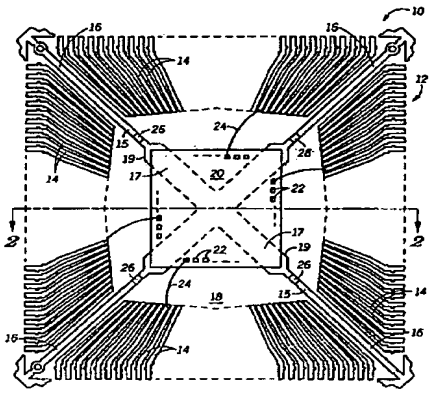


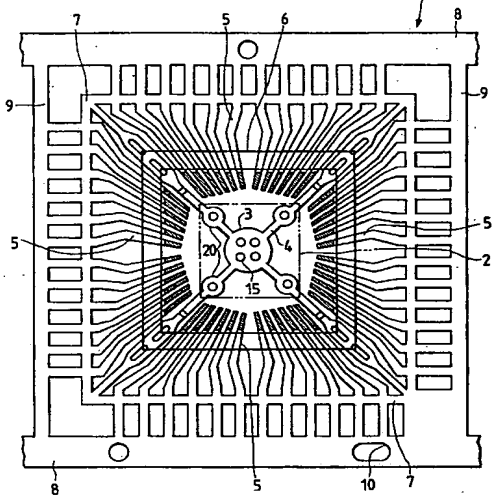
FIG.1

The Office Action recognizes/admits that claims 63-67 distinguish over the art of record, given that no 102/103 rejections are applied within the Office Action against such claims. In conclusion, it is respectfully submitted that such claims 63-67 correct the above-discussed overly-narrow claiming error (*e.g.*, of independent claim 1), while at the same time sufficiently distinguishing over the art of record (*i.e.*, like in the *Eggert* opinion discussed above).

Claims 68-72:

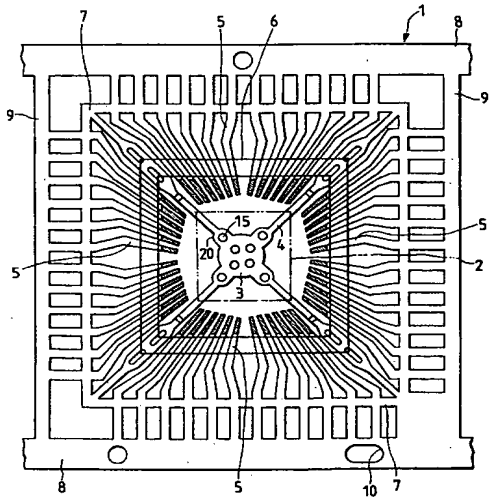
Recapture rebuttal continues with discussion regarding **independent claim 68** (and claims 69-72 dependent therefrom). Review revealed that patented claim 2's limitations may be too narrow, in containing features/limitations: wherein each of said suspension leads includes a first portion (thin/diagonal lead) and a second portion 20 which is wider than said first portion, wherein said second portion (node 20) is **separated from** said chip mounting portion 3 and is positioned under said peripheral portion of said semiconductor chip 2, and wherein said semiconductor chip 2 is fixed at said second portion 20 **of each** of said suspension leads.

FIG. 16



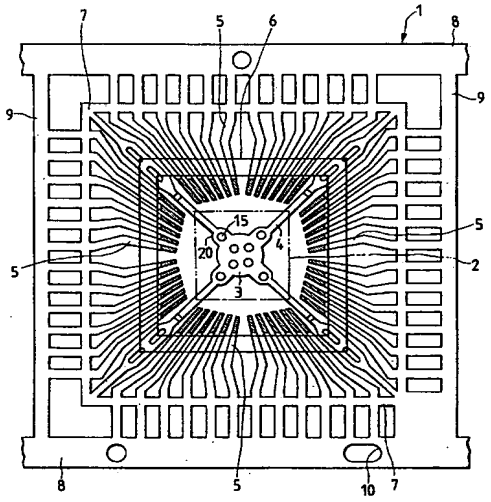
Such claim 2 may be overly limiting with respect to the "separated from" and "each" limitations, as such claim may not cover Applicant's FIG. 15 embodiment which has second portions 20 **not** "separated from" the chip mounted portion 3, and may not cover a potentially infringing arrangement having a semiconductor chip fixed at **LESS THAN "each** of said suspension leads". Accordingly, the "separated from" and "each" limitations are overly-limiting errors within the present patent, which is attempted to be corrected by the present Reissue application.

FIG. 15



Added independent claim 68 avoids such overly-narrow limitations by instead reciting: wherein said chip mounting portion 3 (Applicant's FIG. 15) has **a first portion extending in a first direction** (upper left node 20 to lower right node) and a **second portion extending in a second direction** (lower left node 20 to upper right node) which is a different direction from said first direction, said second portion intersecting said first portion, wherein **a width of each of said first and second portions (nodes 20) of said chip mounting portion is wider** than that of each of said plurality of suspension leads, ...wherein an intersecting portion of said first and second portions of said chip mounting portion is located at a substantially central portion of said rear surface of said semiconductor chip, wherein said both ends of each of said first and second portions of said chip mounting portion are located toward the peripheral portions of said rear surface of said semiconductor chip.

FIG. 15



Further, such claim contains the limitations "wherein said rear surface of said semiconductor chip **is fixed** to said chip mounting portion by an adhesive **at at least two shift-preventing positions separated from each other**", similar to those discussed previously with respect to other groups of Applicant's reissue claims.

To conclude, claim 68 (and claims dependent therefrom) corrects the above-discussed overly-narrow claiming error (*e.g.*, of independent claim 2), while at the same time sufficiently distinguishing over the art of record. That is, none of the references taken alone or in combination would have disclosed or suggested

Applicant's combination of features/limitations as recited in claim 68 (or claims 69-72 dependent therefrom). The Office Action recognizes/admits that claims 68-72 distinguish over the art of record, given that no 102/103 rejections are applied within the Office Action against such claims.

EXTENSIVE PROSECUTION NOTED

Applicant and the undersigned respectfully note the extensive prosecution which has been conducted to-date with the present application, and thus Applicant and the undersigned would gratefully appreciate any considerations or guidance from the Examiner to help move the present application quickly to allowance.

RESERVATION OF RIGHTS

It is respectfully submitted that any and all claim amendments and/or cancellations submitted within this paper and throughout prosecution of the present application are without prejudice or disclaimer. That is, any above statements, or any present amendment or cancellation of claims (all made without prejudice or disclaimer), should not be taken as an indication or admission that any objection/rejection was valid, or as a disclaimer of any scope or subject matter. Applicant respectfully reserves all rights to file subsequent related application(s) (including reissue applications) directed to any/all previously claimed limitations/features which have been subsequently amended or cancelled, or to any/all limitations/features not yet claimed, *i.e.*, Applicant continues (indefinitely) to maintain no intention or desire to dedicate or surrender any limitations/features of subject matter of the present application to the public.

EXAMINER INVITED TO TELEPHONE

The Examiner is invited to telephone the undersigned at the local D.C. area number 703-312-6600, to discuss an Examiner's Amendments or other suggested action for accelerating prosecution and moving the present application to allowance.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that all claims in this reissue application are now in condition for allowance. Accordingly, allowance of all such claims is respectfully requested.

Applicant respectfully petitions the Commissioner for an appropriate extension of the shortened statutory period for response set by the Office Action dated 29 March 2004. A Form PTO-2038 authorizing payment of the requisite Petition and claim fees also is attached hereto. Please charge any deficits in fees to ATS&K Deposit Account No. 01-2135 (as Order No. 501.32049R00).

Respectfully submitted,

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Facsimile 703-312-6666

Attachments:
Appendix
Form PTO-2038 (Fee Codes 1201/1252)

APPENDIX:

[Note: This Appendix is provided solely for convenience; **bolded text** is used to provided guidance and/or indicate changes from Applicant's previously pending claims, and the previously-pending claim numbers 1-36 and 50-72 are used only for convenient reference.]

1. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

2. A semiconductor integrated circuit device according to claim 1, wherein each of said suspension leads includes a first portion and a second portion which is wider than said first portion, wherein said second portion is separated from said chip mounting portion and is positioned under said peripheral portion of said semiconductor chip, and wherein said semiconductor chip is fixed at said second portion of each of said suspension leads.

3. A semiconductor integrated circuit device according to claim 1, wherein said semiconductor chip is of a tetragonal shape.

4. A semiconductor integrated circuit device according to claim 1, wherein said semiconductor chip includes a rear surface opposing said main surface and is fixed to said chip mounting portion and said suspension leads at one portion of said

rear surface, and wherein the other portion of said rear surface which is exposed from said chip counting portion and said suspension leads is directly contacted to said resin member.

5. A semiconductor integrated circuit device according to claim 2, wherein said semiconductor chip is a rectangular shape and said suspension leads include four suspension leads, and wherein four corners of said rectangular-shaped semiconductor chip are supported by said four suspension leads.

6. A semiconductor integrated circuit device according to claim 5, wherein said resin member has a rectangular shape, and wherein said outer lead portions are extended outwardly from four sides of said rectangular-shaped resin member.

7. A semiconductor integrated circuit device according to claim 6, further comprising:

a plurality of grooves for positioning the semiconductor chip, said grooves each formed on said four suspension leads.

8. A semiconductor integrated circuit device according to claim 6, further comprising:

a plurality of projections for positioning the semiconductor chip, said projections each formed on said four suspension leads.

9. A semiconductor integrated circuit device according to claim 7, wherein said grooves are arranged on said four suspension leads so as to accord to four corners of said rectangular-shaped semiconductor chip.

10. A semiconductor integrated circuit device according to claim 8, wherein said projections are arranged on said four suspension leads so as to accord to four corners of said rectangular-shaped semiconductor chip.

11. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

12. A semiconductor integrated circuit device according to claim 11, wherein said semiconductor chip includes a rear surface opposing said main surface and is fixed to said chip mounting portion and said suspension leads at one portion of said rear surface, and wherein the other portion of said rear surface which is exposed from said chip mounting portion and said suspension leads is directly contacted to said resin member.

13. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and

an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

14. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

15. A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion, said first surface of said chip mounting portion being positioned to the side of said second surface of said inner lead portion of each of said plurality of leads rather than the side of said first surface of said inner lead portion of each of said plurality of leads;

(b) mounting a semiconductor chip on said chip mounting portion, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion, said semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(c) electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires respectively, in condition that said lead frame is placed on a heat stage having a groove for accommodating said chip mounting portion and said suspension leads and for a wire bonding operation, wherein said connecting step is performed in a condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is in contact with an upper surface of said heat stage and said second surface of said chip mounting portion its spaced from a bottom surface of said groove; and

(d) sealing said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

16. A method of manufacturing a semiconductor device according to claim 15, wherein the step (a) includes bending said suspension leads, and wherein a depth of said groove is deeper than a level of said bending of said suspension leads.

17. A method of manufacturing a semiconductor device according to claim 15, wherein the step (b) includes providing an adhesive to said first surface of said chip mounting portion, wherein said semiconductor chip and said chip mounting portion are bonded to each other by said adhesive.

18. A method of manufacturing a semiconductor device according to claim 17, wherein said adhesive is not provided to said suspension leads.

19. A method of manufacturing a semiconductor device according to claim 15, wherein said plurality of leads has a first lead adjacent to one of said suspension leads and a second lead which is relatively far from said one of said suspension leads in comparison with said first lead, and wherein a distance between the tip of said first lead and an edge of said semiconductor chip is shorter than a distance between the tip of said second lead and said edge of said semiconductor chip.

20. A method of manufacturing a semiconductor device according to claim 19, wherein a length of bonding wire connected to said first lead is shorter than a length of bonding wire connected to said second lead.

21. A method of manufacturing a semiconductor device according to claim 15, wherein a width of said chip mounting portion is larger than that of each of said suspension leads.

22. A method of manufacturing a semiconductor device according to claim 15, wherein in the step (c), parts of said inner lead portions of said plurality of leads, to which said plurality of bonding wires are bonded, are placed on said upper surface of said heat stage.

23. A method of manufacturing a semiconductor device according to claim 15, wherein said chip mounting portion has a substantially circular form in a plane view.

24. A method of manufacturing a semiconductor device according to claim 15, wherein said chip mounting portion has a substantially cross form in a plane view.

25. A method of manufacturing a semiconductor device comprising the steps of :

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion;

(b) preparing a semiconductor chip selected from among a plurality of semiconductor chips having different sizes, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion; (c) mounting said semiconductor chip on said chip mounting portion, said semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(d) electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires, in a condition that said lead frame is placed on a heat stage having a groove for accommodating said chip mounting portion and said suspension leads and for a wire bonding operation, wherein said connecting step is performed in condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is contact with an upper surface of said heat stage and said second surface of said chip mounting portion is spaced from a bottom surface of said groove; and

(e) sealing said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

26. A method of manufacturing a semiconductor device according to claim 25, further comprising a step of bending said suspension leads such that said first surface of said chip mounting portion is located on a down side than said first surface of said inner lead portion of each of said plurality of leads in a thickness direction of said lead frame.

27. A method of manufacturing a semiconductor device according to claim 26, wherein said bending step includes providing a step portion to each of said suspension leads by said bending, and wherein a depth of said groove is deeper than a level of said bending of said suspension leads.

28. A method of manufacturing a semiconductor device according to claim 25, wherein the step (c) includes providing an adhesive to said first surface of said chip mounting portion, wherein said semiconductor chip and said chip mounting portion are bonded to each other by said adhesive.

29. A method of manufacturing a semiconductor device according to claim 28, wherein said adhesive is not provided to said suspension leads.

30. A method of manufacturing a semiconductor device according to claim 25, wherein said plurality of leads has a first lead adjacent to one of said suspension leads and a second lead which is relatively far from said one of said suspension leads in comparison with said first lead, and wherein a distance between the tip of

said first lead and an edge of said semiconductor chip is shorter than a distance between the tip of said second lead and said edge of said semiconductor chip.

31. A method of manufacturing a semiconductor device according to claim 30, wherein a length of bonding wire connected to said first lead is shorter than a length of bonding wire connected to said second lead.

32. A method of manufacturing a semiconductor device according to claim 25, wherein a width of said chip mounting portion is larger than that of each of said suspension leads.

33. A method of manufacturing a semiconductor device according to claim 25, wherein in the step (e), parts of said inner lead portions of said plurality of leads, to which said plurality of bonding wires are bonded, are placed on said upper surface of said heat stage.

34. A method of manufacturing a semiconductor device according to claim 25, wherein said chip mounting portion has a substantially circular form in a plane view.

35. A method of manufacturing a semiconductor device according to claim 25, wherein said chip mounting portion has a substantially cross form in a plane view.

36. A method of manufacturing a semiconductor device comprising the steps of;

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion, said first surface of said chip mounting portion being positioned to the side of said second surface of said inner lead portion of each of said plurality of leads rather than the side of said first surface of said inner lead portion of each of said plurality of leads;

(b) mounting a semiconductor chip on said chip mounting portion, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion, said semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(c) electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires respectively, in condition that said lead frame is placed on a heat stage having a groove for accommodating said chip mounting portion and said suspension leads and for a wire bonding operation, wherein said connecting step is performed in a condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is in contact with an upper

surface of said heat stage and said second surface of said chip mounting portion and said suspension leads are spaced from a bottom surface of said groove; and

(d) sealing said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

37-49. (Canceled)

50. A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion for mounting said semiconductor chip;

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and arranged at a periphery of said chip mounting portion;

suspension leads continuously formed with said chip mounting portion, said semiconductor chip being mounted on said chip mounting portion;

(c) an insulating tape adhered to said inner lead portions of said plurality of leads and said suspension leads;

(d) bonding wires electrically connected to said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively, and

(e) a resin member sealing said semiconductor chip, said bonding wires, said insulating tape, said chip mounting portion, a part of each of said suspension leads, and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip, and

wherein said insulating tape continuously extends from said inner lead portions of said plurality of leads to said suspension leads.

51. A semiconductor device according to claim 50, wherein said resin member has a rectangular shape, wherein said suspension leads extend from said chip mounting portion toward four corners of said resin member, and wherein said inner lead portions of said plurality of leads are arranged between said suspension leads in a plane view.

52. A semiconductor device according to claim 50, wherein said insulating tape extends along four sides of said resin member to surround said chip mounting portion and said semiconductor chip in a plane view.

53. A semiconductor device according to claim 50, wherein said insulating tape includes a base insulating film and an adhesive layer applied to one surface of said base insulating film, and wherein said insulating tape is adhered to said inner lead portions and said suspension leads by said adhesive layer.

54. A semiconductor device according to claim 53, wherein said base insulating film includes a polyimide resin and said adhesive layer includes an acrylic resin.

55. A semiconductor device according to claim 50, wherein said lead frame having a first surface and a second surface opposite to said first surface, wherein each of said suspension leads has a step portion so that said first surface of said chip mounting portion is positioned to the side of said second surface of said inner lead portion of each of said plurality of leads rather than the side of said first surface of said inner lead portion of each of said plurality of leads, and wherein said insulating tape is arranged outside said step portion of each of said suspension leads.

56. A semiconductor device according to claim 55, wherein a part of each of said suspension leads, which is located outside said step portion, is substantially at a same level as said inner lead portions of said plurality of leads in a thickness direction of said lead frame.

57. A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface;

(b) a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads continuously formed with said chip mounting portion;

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at a periphery of said chip mounting portion;

(c) a plurality of bonding wires electrically connected to said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively; and

(d) a resin member sealing said semiconductor chip, said bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said semiconductor chip is mounted on said chip mounting portion, such that said rear surface of said semiconductor chip is bonded to the side of said first surface of said chip mounting portion by an adhesive layer, and such that a part of each of said suspension leads, which is located under said semiconductor chip, is spaced from said rear surface of said semiconductor chip.

58. A semiconductor device according to claim 57, wherein said adhesive layer is provided on said first surface of said chip mounting portion and is not provided on said part of each of said suspension leads which is located under said semiconductor chip.

59. A semiconductor device according to claim 58, wherein a part of said rear surface of said semiconductor chip, which is located outside said chip mounting portion, is adhered to a part of said resin member.

60. A semiconductor device according to claim 59, wherein said resin member includes a thermosetting resin.

61. A semiconductor device according to claim 57, wherein said adhesive layer includes an epoxy resin.

62. A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface;

(b) a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads continuously formed with said chip mounting portion;

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at the periphery of said chip mounting portion;

(c) a plurality of bonding wires electrically connected to said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively; and

(d) a resin member sealing said semiconductor chip, said bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said semiconductor chip is bonded to said chip mounting portion by an adhesive layer between said rear surface of said semiconductor chip and said first surface of said chip mounting portion,

wherein each of said suspension leads has a part which is located under said semiconductor chip, and

wherein a part of said resin member is formed between said part of each of said suspension leads and said rear surface of said semiconductor chip.

63. **(Amendments from prior version indicated in bold)** A semiconductor device comprising:

(1) a semiconductor chip having a main surface and a rear surface opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface;

(2) a lead frame including:

a first suspension lead for supporting said semiconductor chip, extending in a first direction;

a second suspension lead for supporting said semiconductor chip, extending in a second direction which is different from said first direction, said second suspension lead intersecting said first suspension lead; and

a plurality of leads each having an inner lead and an outer lead which is continuously formed with said inner lead, said plurality of leads being arranged to surround an intersecting portion of said first and second suspension leads;

(3) a plurality of bonding wires electrically connecting said inner leads of said plurality of leads with said plurality of bonding pads, respectively; and

(4) a resin body sealing said semiconductor chip, said inner leads of said plurality of leads, said first and second suspension leads and said plurality of bonding wires;

wherein said semiconductor chip is disposed on **and supported by a flag-less** said intersecting portion of said first and second suspension leads, **with said first and second suspension leads being unitarily formed with one another**,

wherein a width of each of said first and second suspension leads **supporting said semiconductor chip** at the vicinity of said intersecting portion is wider than that of each said first and second suspension leads at vicinities beyond said semiconductor chip, **and widened portions of said first and second suspension leads are smaller than said semiconductor chip,** and

wherein said rear surface of said semiconductor chip is fixed to said first and second suspension leads **by an adhesive at at least two shift-preventing positions separated from each other.** ~~**at the vicinity of said intersecting point by an adhesive.**~~

64. A semiconductor device according to claim 63, wherein said first and second suspension leads intersect each other at a substantially right angle.

65. A semiconductor device according to claim 64, wherein said resin body has a tetragonal shape, wherein said outer leads of said plurality of leads protrude outwardly from four sides of said resin body, and wherein said first and second

suspension leads extend from said intersecting portion toward four corners of said resin body.

66. A semiconductor device according to claim 63, wherein a portion of said rear surface of said semiconductor chip is adhered to said intersecting portion of said first and second suspension leads, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

67. A semiconductor device according to claim 64, wherein said semiconductor chip has a tetragonal shape, and wherein said wider portion at the vicinity of said intersecting portion of said first and second suspension leads extends from a central portion of said rear surface of said semiconductor chip toward four corners of said semiconductor chip.

68. **(Amendments from prior version indicated in bold)** A semiconductor device comprising:

(1) a semiconductor chip having a main surface and a rear surface opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface;

(2) a lead frame including:

a chip mounting portion for mounting said semiconductor chip, **wherein said chip mounting portion is smaller than said semiconductor chip**;

a plurality of suspension leads which are ~~continuously~~ **unitarily** formed with said chip mounting portion; and

a plurality of leads each having an inner lead and an outer lead which is continuously formed with said inner lead, said plurality of leads being arranged to surround said chip mounting portion;

(3) a plurality of bonding wires electrically connecting said inner leads of said plurality of leads with said plurality of bonding pads, respectively; and

(4) a resin body sealing said semiconductor chip, said inner leads of said plurality of leads, said chip mounting portion, said plurality of suspension leads and said plurality of bonding wires;

wherein said chip mounting portion has a first portion extending in a first direction and a second portion extending in a second direction which is a different direction from said first direction, said second portion intersecting said first portion,

wherein a width of each of said first and second portions of said chip mounting portion is wider than that of each of said plurality of suspension leads,

wherein both ends of each of said first and second portions of said chip mounting portion are coupled with said plurality of suspension leads respectively,

wherein an intersecting portion of said first and second portions of said chip mounting portion is located at a substantially central portion of said rear surface of said semiconductor chip,

wherein said both ends of each of said first and second portions of said chip mounting portion are located **at toward** the peripheral portions of said rear surface of said semiconductor chip, and

wherein said rear surface of said semiconductor chip is fixed to said chip mounting portion **by an adhesive at at least two shift-preventing positions**

separated from each other. ~~at both of said central and peripheral portions of said rear surface of said semiconductor chip by an adhesive.~~

69. A semiconductor device according to claim 68, wherein said first and second directions intersect each other at a substantially right angle.

70. A semiconductor device according to claim 69, wherein said resin body has a tetragonal shape, wherein said outer leads of said plurality of leads protrude outwardly from four sides of said resin body, and wherein said plurality of suspension leads extend from said both ends of said first and second portions of said chip mounting portion toward four corners of said resin body.

71. A semiconductor device according to claim 68, wherein a portion of said rear surface of said semiconductor chip is adhered to said first and second portions of said chip mounting portion, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

72. A semiconductor device according to claim 71, wherein said semiconductor chip has a tetragonal shape, and wherein said both ends of each of said first and second portions are located at the vicinity of four corners of said semiconductor chip.

73. **(Substantially parallels claim 1; differences indicated in bold)** A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of ~~each~~ **at least one** of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of ~~each~~ **said at least one** of said suspension leads and said semiconductor chip are **positionally** separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

74. **(Substantially parallels claim 11; differences indicated in bold)** A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of **~~each~~ at least one** of said suspension leads by adhesive which is located under a peripheral portion of said

semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of **~~each~~ said at least one** of said suspension leads and said semiconductor chip are **positionally** separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

75. **(Substantially parallels claim 13; differences indicated in bold)** A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip,

said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of ~~each~~ **at least one** of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and

an adhesive region of ~~each~~ **said at least one** of said suspension leads and said semiconductor chip are **positionally** separated from each other.

76. **(Substantially parallels claim 14; differences indicated in bold)** A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

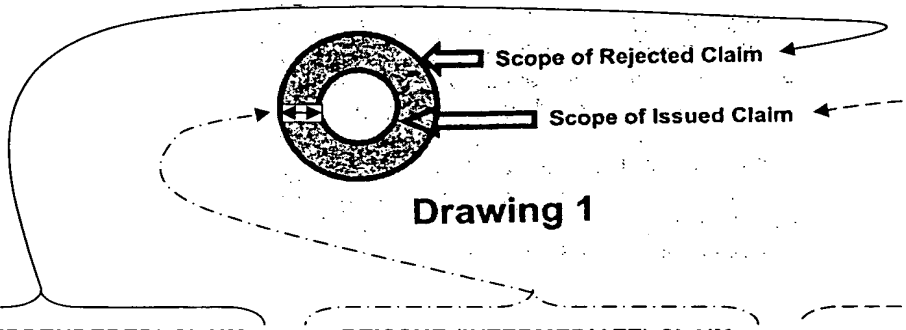
a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of **~~each~~ at least one** of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of **~~each~~ said at least one** of said suspension leads and said semiconductor chip are **positionally** separated from each other.

EGGERT ANALYSIS



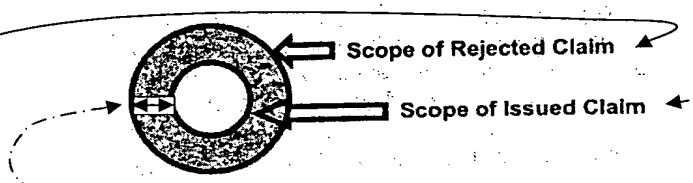
Drawing 1

REJECTED (SURRENDERED) CLAIM Eggert's Independent claim 1 after first amendment of interest (additions in italics)	**REISSUE (INTERMEDIATE) CLAIM** Eggert's reissue claim 15 (compared to issued claim 1; deletions in strikeout; additions in underline)	**ISSUED CLAIM** Eggert's issued independent claim 1 of '426 patent
A bit holder comprising:	A bit holder comprising:	A bit holder comprising:
a cylindrical body having a distal end surface and an axis, said body having formed in said end surface an axial bore terminating at an inner end surface,	a ~~cylindrical~~ body having a distal end surface ~~and an axis~~, said body having a bore formed in said end surface ~~an axial bore terminating at an inner end surface~~,	a cylindrical body having a distal end surface and an axis, said body having formed in said end surface an axial bore terminating at an inner end surface,
a permanent magnet received in said bore and having an outer surface, and	a ~~permanent~~ magnet received in said bore and having an outer surface, and	a permanent magnet received in said bore and having an outer surface, and
retaining structure in contact with the outer surface of said magnet and interference fitted in said bore to retain said magnet in said bore,	a discrete retaining ~~structure in contact with the outer surface of said magnet and interference~~ member friction fitted in said bore outboard of said magnet and substantially covering said outer surface of said magnet to retain said magnet in said bore,	retaining structure in contact with the outer surface of said magnet and interference fitted in said bore to retain said magnet in said bore,
said bore having a portion of non-circular transverse cross section outboard of said retaining structure defining a bit-receiving socket	said bore having a portion ~~of non-circular transverse cross section~~ outboard of said retaining ~~structure~~ member defining a bit-receiving socket.	said bore having a portion of non-circular transverse cross section outboard of said retaining structure defining a bit-receiving socket
said retaining structure including a discrete retaining member friction fitted in said bore outboard of said magnet,	~~*said retaining structure including a discrete retaining member friction fitted in said bore outboard of said magnet,*~~	*said retaining structure including a discrete retaining member friction fitted in said bore outboard of said magnet,*
	~~*said retaining member being generally bowl-shaped and convex towards said magnet,*~~	~~*said retaining member being generally bowl-shaped and convex towards said magnet,*~~
said retaining member and said inner end surface cooperating to retain said magnet therebetween.	~~*said retaining member and said inner end surface cooperating to retain said magnet therebetween.*~~	*said retaining member and said inner end surface cooperating to retain said magnet therebetween.*

KEY:
Reasons for allowance

Alleged recapture areas

PRESENT APPLICATION ANALYSIS



Drawing 1

REJECTED (SURRENDERED) CLAIM Original independent claim 25 of the '992 application:	REISSUE (INTERMEDIATE) CLAIM New claim 73 of reissue application (compared to issued claim 1; deletions in strikeout; additions in underline)	ISSUED CLAIM issued independent claim 1 of '913 patent
25. A semiconductor integrated circuit device comprising:	73. A semiconductor integrated circuit device comprising:	1. A semiconductor integrated circuit device comprising:
a semiconductor chip having a principal surface including semiconductor elements and a plurality of bonding pads;	a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;	a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;
a leadframe having	a leadframe having:	a leadframe having:
a chip mounting portion for mounting said semiconductor chip,	a chip mounting portion for mounting said semiconductor chip;	a chip mounting portion for mounting said semiconductor chip;
suspension leads unitarily formed with said chip mounting portion,	suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,	suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,
a plurality of inner lead portions arranged to surround said semiconductor chip, said inner lead portions are electrically connected with said bonding pads, and	a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and	a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and
a plurality of outer lead portions individually connected with said inner lead portions; and	a plurality of outer lead portions individually connected with said inner lead portions; and	a plurality of outer lead portions individually connected with said inner lead portions; and
a resin member sealing said semiconductor chip, said inner lead portions and said chip mounting portion and said suspension leads;	a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;	a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;
wherein said chip mounting portion is smaller than said principal surface of said semiconductor chip and said semiconductor chip is fixed to a part of said suspension leads and said chip mounting portion.	wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part ~~of each at least one of~~ said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region ~~of each at least one of~~ said suspension leads and said semiconductor chip are positionally separated from each other and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an ~~area~~ of said semiconductor chip.	wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

KEY:
Reasons for allowance

Alleged recapture areas